CUSTOMER APPROVAL SHEET

Company Name	
MODEL	**A060SE02 V5**
CUSTOMER APPROVED	

- ☐ APPROVAL FOR SPECIFICATIONS ONLY (Spec. Ver. 0.2)
- ☐ APPROVAL FOR SPECIFICATIONS AND ES SAMPLE (Spec. Ver. 0.2)
- ☐ APPROVAL FOR SPECIFICATIONS AND CS SAMPLE (Spec. Ver. 0.2)
- ☐ CUSTOMER REMARK :

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Product Specification

6" EPD with touch panel MODULE

Model Name : A060SE02 V5

Planned Lifetime:	From 2010/May. To 2011/May.
Phase-out Control:	From 2011/Feb. To 2011/May.
EOL Schedule:	2011/May.

< ◆ >Preliminary Specification
< >Final Specification

Note: The content of this specification is subject to change.

Record of Revision

Version	Revise Date	Page	Content
0.0	2010/05/19	All	First Draft.
0.1	2010/6/10	0	Modify Life Time, phase out control and EOL Time
		3	Modify general information, overall dimension, and number of gray levels.
		10	Add item “Image Update Time” to “D. Electrical Characteristic”
		10	Update power consumption format
		17	Update power on/off sequence
		18, 19	Modify value of “Reflectance” and remark Modify value of “Contrast Ratio” and remark Modify item “Response Time” to “Update Time”, Remove definition of “Response Time”
		20, 21	Add Reliability Test Item “UV Exposure Resistance”, remove some items and modify remarks and notes
		26	Add precaution items 19~21.
		30	Update INT_SETTING default value
0.2	2010/7/13	10	Update typical power consumption measured pattern
		20,21	Reliability Test Items number typo modify
		26	Add precaution items 22,23

Contents

A. General Information

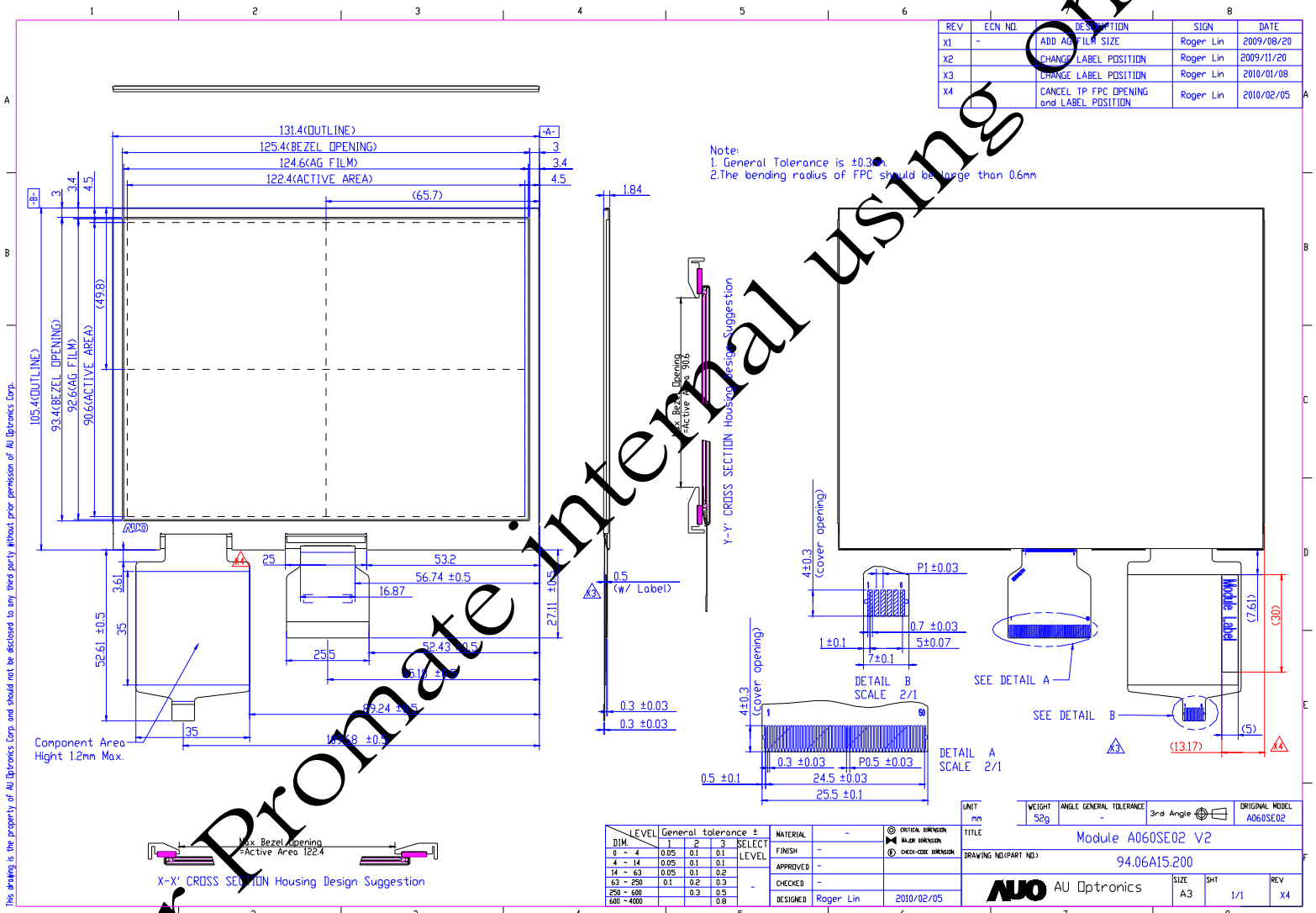
This display is a active matrix electrophoretic display (EPD), which comprises a-si TFT substrace, electrophoretic front plane, protective anti-glare top-sheet, driver ICs, and FPC. It is designed for applications such as e-book or e-reader.

NO.	Item	Unit	Specification	Remark
1	Screen Size	inch	6 (Diagonal)	
2	Display Resolution	dot	800 (H)× 600(V)	
3	Overall Dimension	mm	131.4(H) × 105.39(V) × (1.84) (T)	Note 1
4	Active Area	mm	122.4(H)×90.6(V)	
5	Dot Pitch	mm	0.153 (H)x 0.151(V)	
6	Gray Level	--	8	
7	Weight	g	(52)	
8	Surface Treatment		AG (7.5 ± 2%) Hard coating (3H)	Note 2

Note 1: Not include FPC and label. Refer to next page to get further information.

Note 2: 750 g load force on UNI/JPIA 3H pencil, speed is 3.5mm/s on the AG film and scratch length is 1cm and write 5 handwriting, Scratch no. ≦2 is OK

B. Outline Dimension



C. Electrical Specifications

1. Pin Assignment

Recommended connector : FH12-50S-0.5SH.

Pin No.	Symbol	I/O	I/O Structure	Description	Remark
1	Dummy	--	--	Dummy pin	
2	VCOM	O	--	VCOM polarity output signal	
3	VCOM_BOT	I	--	VCOM signal setting pin	
4	VCOMDC	P	Type2	External voltage for VCOMDC power.	
5	VCOMH	P	--	External voltage for VCOM high power.	
6	VCOML	P	--	External voltage for VCOM low power.	
7	RST_N	I	Type 3	Global reset pin. Low reset.	
8	SHD_N	I	Type 3	DC-DC converter shut down pin. "0" : Enable.(Panel shut down;**Default**) "1" : Disable.	
9	PWR_RDY	O	Type 1	Power ready output. When SHD_N from "1" to "0": PWR_RDY will become "0". When SHD_N from "0" to "1": after 100ms, PWR_RDY will become "1".	Note1
10	VCOMIN_0	I	Type 2	Logic Input for VCOM voltage generate.	
11	VCOMIN_1	I	Type 2	Logic Input for VCOM voltage generate.	
12	YOE	I	Type 3	Vertical output enable pin.	Note2
13	YCLK	I	Type 3	Vertical clock. Input	Note2
14	UD	I	Type 3	Vertical (up/down) scan direction. U/D = "L": Shift up to down. **Default** U/D = "H": Shift down to up.	

<table>
<tr><td>15</td><td>YDIOD</td><td>I/O</td><td>Type 5</td><td rowspan="2">Vertical start pulse input/output.
These pins are used to input and output shift data. These pins are switched as input or output by setting the UD pin as follow.
<table><tr><th>UD</th><th>YDIOU</th><th>YDIOD</th></tr><tr><td>L</td><td>Output</td><td>Input</td></tr><tr><td>H</td><td>Input</td><td>Output</td></tr></table></td><td rowspan="2"></td></tr>
<tr><td>16</td><td>YDIOU</td><td>I/O</td><td>Type 5</td></tr>
<tr><td>17</td><td>XDIOL</td><td>I/O</td><td>Type 5</td><td rowspan="2">Horizontal start pulse input/output.
These pins are used to input and output shift data. These pins are switched as input or output by setting the SHL pin as follow.
<table><tr><th>SHL</th><th>XDIOL</th><th>XDIOR</th></tr><tr><td>L</td><td>Input</td><td>Output</td></tr><tr><td>H</td><td>Output</td><td>Input</td></tr></table></td><td rowspan="2"></td></tr>
<tr><td>18</td><td>XDIOR</td><td>I/O</td><td>Type 5</td></tr>
<tr><td>19</td><td>LD</td><td>I</td><td>Type 3</td><td>Latch data.</td><td></td></tr>
<tr><td>20</td><td>D0</td><td>I</td><td>Type 3</td><td>Data input, First pixel LSB</td><td></td></tr>
<tr><td>21</td><td>D1</td><td>I</td><td>Type 3</td><td>Data input, First pixel MSB</td><td></td></tr>
<tr><td>22</td><td>D2</td><td>I</td><td>Type 3</td><td>Data input, Second pixel LSB</td><td></td></tr>
<tr><td>23</td><td>D3</td><td>I</td><td>Type 3</td><td>Data input, Second pixel MSB</td><td></td></tr>
<tr><td>24</td><td>D4</td><td>I</td><td>Type 3</td><td>Data input, Third pixel LSB</td><td></td></tr>
<tr><td>25</td><td>D5</td><td>I</td><td>Type 3</td><td>Data input, Third pixel MSB</td><td></td></tr>
<tr><td>26</td><td>D6</td><td>I</td><td>Type 3</td><td>Data input, Forth pixel LSB</td><td></td></tr>
<tr><td>27</td><td>D7</td><td>I</td><td>Type 3</td><td>Data input, Forth pixel MSB</td><td></td></tr>
<tr><td>28</td><td>SHL</td><td>I</td><td>Type 3</td><td>Horizontal (left/right) scan direction.
SHL = “L”: Shift right to left.
SHL = “H”:Shift left to right. Default</td><td></td></tr>
<tr><td>29</td><td>XCLK</td><td>I</td><td>Type 3</td><td>Horizontal Clock input..</td><td>Note3</td></tr>
<tr><td>30</td><td>VREF</td><td>C</td><td>--</td><td>For power setting capactor connected pin.</td><td></td></tr>
<tr><td>31</td><td>VR</td><td>P</td><td>--</td><td>VCOMDC reference voltage</td><td></td></tr>
<tr><td>32</td><td>AVDD</td><td>C</td><td>--</td><td>For power setting capactor connected pin.</td><td></td></tr>
<tr><td>33</td><td>C1P</td><td>C</td><td>--</td><td>For charge pump capactor connected pin.</td><td></td></tr>
<tr><td>34</td><td>C1N</td><td>C</td><td>--</td><td>For charge pump capactor connected pin.</td><td></td></tr>
<tr><td>35</td><td>VSS</td><td>P</td><td>--</td><td>Digital ground</td><td></td></tr>
<tr><td>36</td><td>VSSA</td><td>P</td><td>--</td><td>Analog ground.</td><td></td></tr>
<tr><td>37</td><td>VDD</td><td>P</td><td>--</td><td>Analog power.</td><td></td></tr>
<tr><td>38</td><td>VREF_POS</td><td>C</td><td>--</td><td>For power setting capactor connected pin.</td><td></td></tr>
<tr><td>39</td><td>VREF_NEG</td><td>C</td><td>--</td><td>For power setting capactor connected pin.</td><td></td></tr>
</table>

40	VDDX8	P	--	DCDC positive voltage	
41	NVDDX8	P	--	DCDC negative voltage	
42	VDD_DRV	P	--	DCDC power.	
43	ADRVU	O	Type 1	PWM output for DCDC converter.	
44	ADRVD	O	Type 1	PWM output for DCDC converter.	
45	VSS_DRV	P	--	DCDC ground.	
46	VDPS	P	--	External voltage for source postive power.	
47	VDNS	P	--	External voltage for source negative power.	
48	VDPG	C	--	For power setting capactor connected pin.	
49	VDNG	C	--	For power setting capactor connected pin.	
50	Dummy	D	--	Dummy pin	

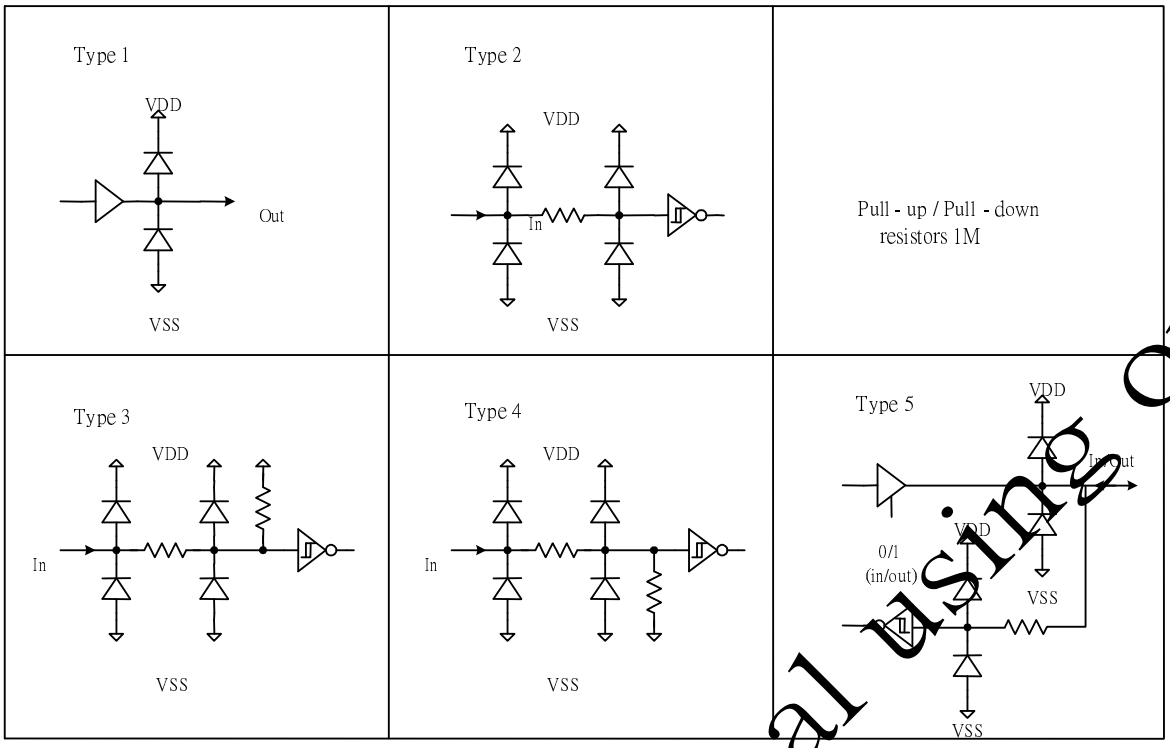
I: Input pin; O:output pin, I/O: Input / Output; P: Power pin; C: capacitor pin; D：Dummy

Note 1: Please reference chapter F

Note 2: Please reference chapter E

Note 3: Please reference chapter E

I/O Pin Structure:



2. Touch Panel Pin Assignment

Pin No.	Symbol	I/O	Description	Remark
1	GND	P	Touch panel ground.	
2	VDD_TP	P	Touch panel power.	
3	TP_INT	O	Touched Interrupt Indicator pin.	
4	IICSCL	I	Serial input clock in I2C-Bus interface operation pin.	
5	IICSDA	I/O	Serial input/output data in I2C-Bus interface operation pin.	
6	RST_TP	I	Touch panel reset pin.	

3. Absolute Maximum Ratings

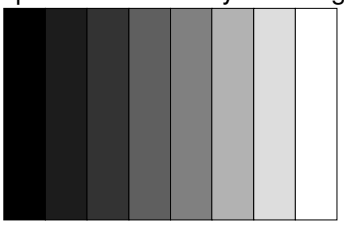
Item	Symbol	Condition	Min.	Max.	Unit	Remark
Power voltage	VDD	VSSA=VSS=0	-0.3	+5.0	V	
Power voltage	VDD_DRV	VSS_DRV=0	-0.3	+5.0	V	
Source voltage	VDPS	VSSA=VSS=0		+20	V	
	VDNS	VSSA=VSS=0	-20		V	
Gate voltage	VDPG	VSSA=VSS=0	+0.3	VDNG+40		
	VDNG	VSSA=VSS=0	VDPG-40	+0.3		
Storage temperature	Tstg	-	-25	70	℃	
Operating	Topa	-	0	50	℃	

D. Electrical Characteristics

1. Panel Power Consumption

Item	Symbol	Condition	Min.	Typical	Max.	Unit
Supply Voltage	VDD	VSSA=VSS=VSS_DRV=0V	--	3.3	--	V
	VDD_DRV	VSSA=VSS=VSS_DRV=0V	--	3.3	--	
Touch Panel Supply Voltage	VDD_TP	VSSA=VSS=VSS_DRV=0V	-	3.3	-	V
Low Level Input Voltage	Vil	Digital input pins	GND	-	0.3xVDD	V
High Level Input Voltage	Vih	Digital input pins	0.7xVDD	-	VDD	V
Operating temperature	T_{op}		-	25	-	℃
Operation Power Dissipation	P	VDD=VDD_DRV=3.3V	--	1.07	2	mA
		VDNS=-15V		0.82	1.5	mA
		VDPS=15V		0.86	1.5	mA
		VDPG=20V		1.23	2	mA
		VDNG=-20V		0.66	1.5	mA
		VCOMH=12V		0.36	1	mA
		VCOML=-18V		0.56	1	mA
Standby Power Dissipation	P	VDD=VDD_DRV=3.3V	--	0.06	0.15	mA
		VDNS=0V		0.02	0.1	mA
		VDPS=0V		0.02	0.1	mA
		VDPG=3.3V		0.02	0.1	mA
		VDNG=0V		0.02	0.1	mA
		VCOMH=0V，		0.01	0.1	mA
		VCOML=0V		0.02	0.1	mA
Image Update Time		T=25℃	--	950	1010	ms
		T=10℃	--	2310	2450	ms
		T=0℃	--	2750	3150	ms

*: Typical power consumption measured by following pattern



2. Touch Panel Power Consumption

Mode	Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Active	Ptp_a	VDD= 3.0V	-	(9)	-	mA	
Sleep	Ptp_s		-	(1)	-	mA	
Deep Sleep	Ptp_dp		-	(0.7)	-	mA	

E. Input timing AC Characteristics

1. Horizontal input timing

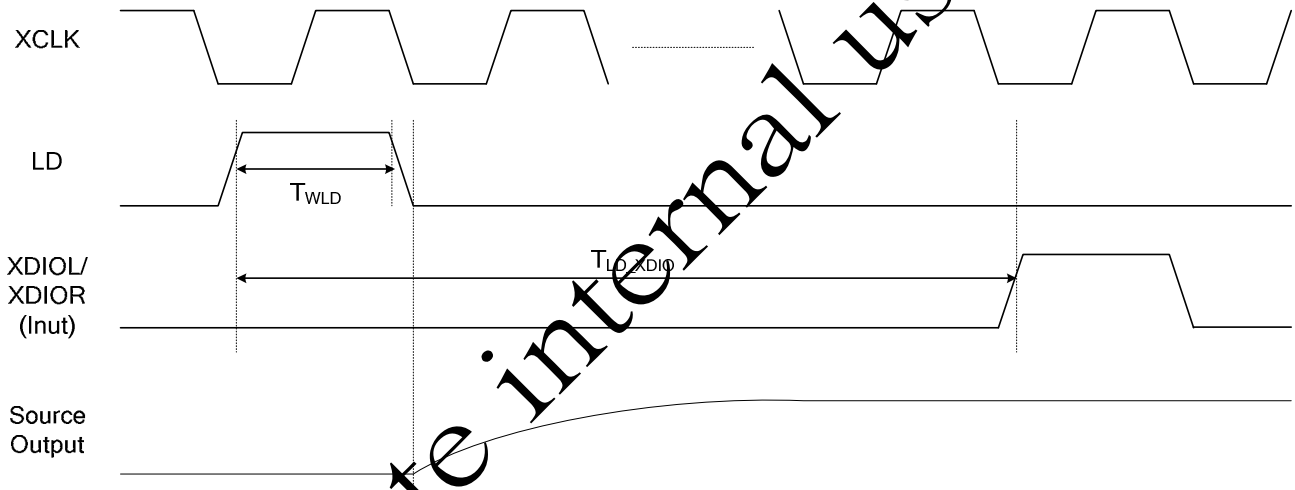


Figure 1: LD input timing

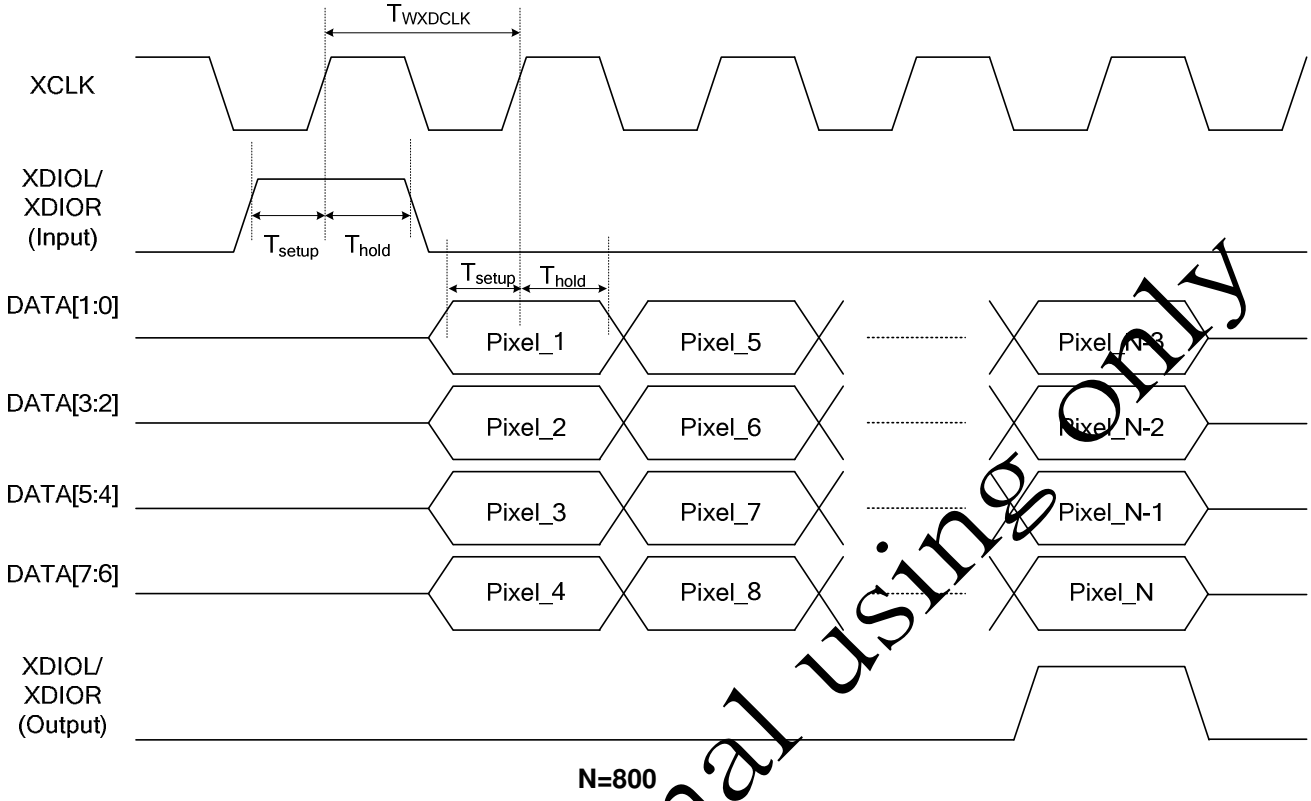


Figure 2: Horizontal data input timing

(VDD=VDD_DRV=3.3V, VSSA=VSS=VSS_DRV=0V, TA=25℃)

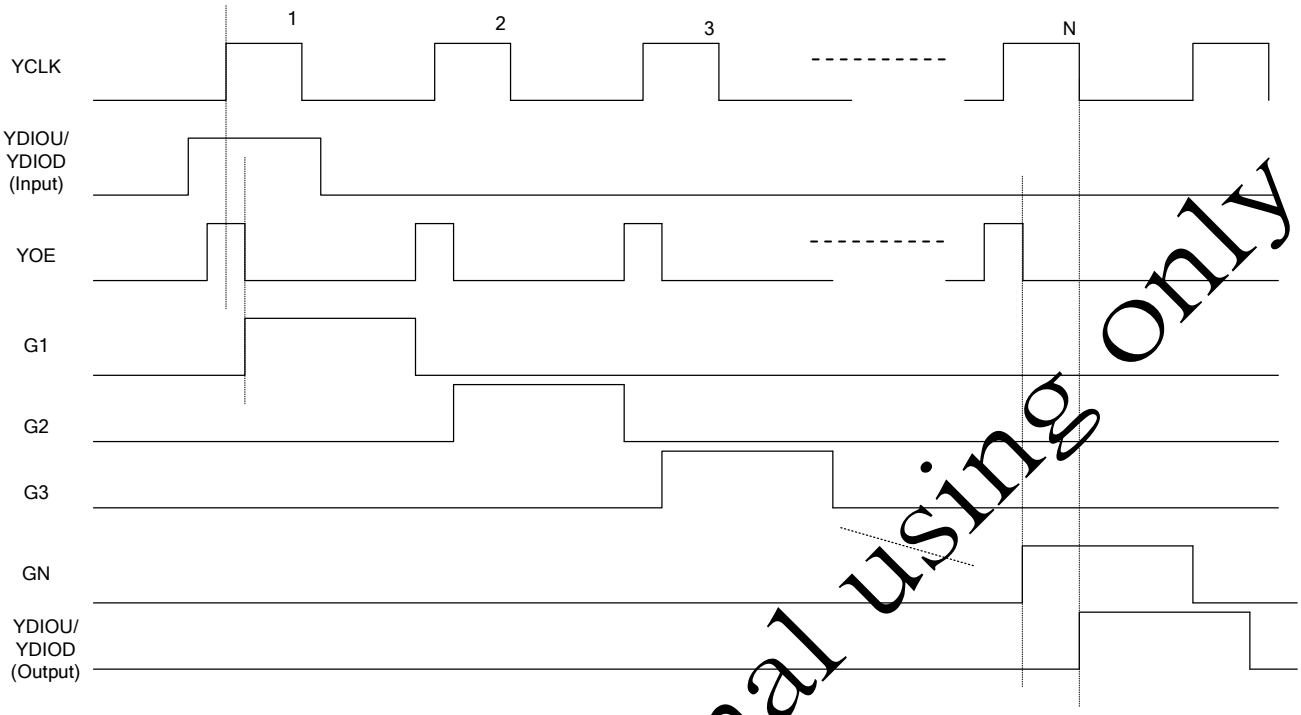
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Clock pulse width	T_{WXDCLK}	13			ns
Data setup time	T_{setup}	2	-	-	ns
Data hold time	T_{hold}	2	-	-	ns
LD pulse width	T_{WLD}	1	-	-	XCLK
Time from LD to XDIOL/XDIOR	T_{LD_DIO}	5	-	-	XCLK

1.1 Relationship of input data and source output voltage

The source driver output voltage will base on input 2 bits data, and the relationship is as below:

MSB	LSB	Function
0	0	Source output is 0V
0	1	Source output is VDPS(+15V)
1	0	Source output is VDNS(-15V)
1	1	Source output is floating

2. Vertical input timing



N=600

Figure 3: Vertical input timing

3. VCOM voltage definition

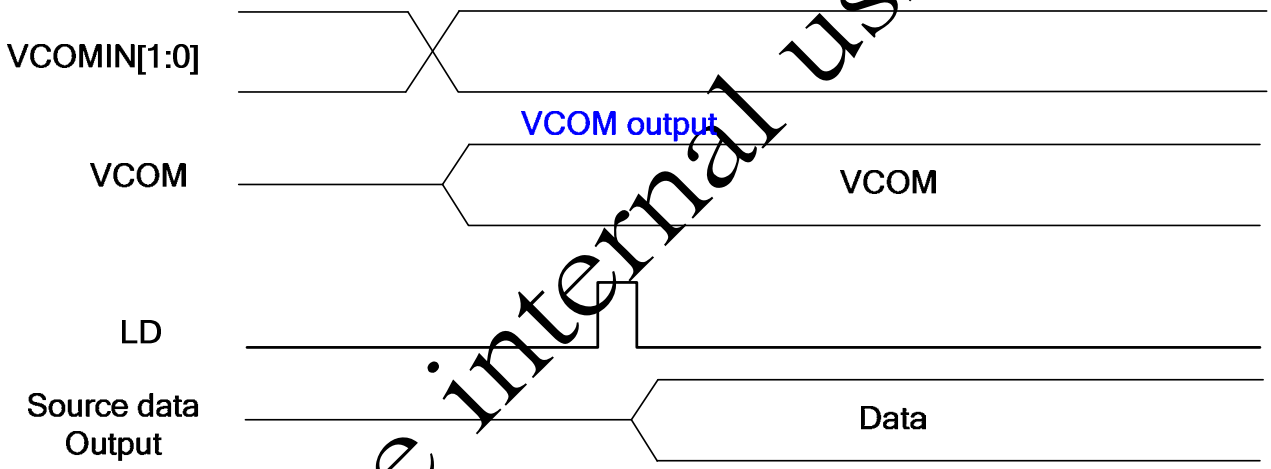
The VCOM output voltage will base on input pins VCOMIN[1:0], and the relationship is as below:

VCOMIN[1 :0]	Function
00	VCOM output is (-VDC) v
01	VCOM output is (VDPS-VDC) v
10	VCOM output is (VDNS-VDC) v
11	VCOM output is floating

4. VCOM relationship

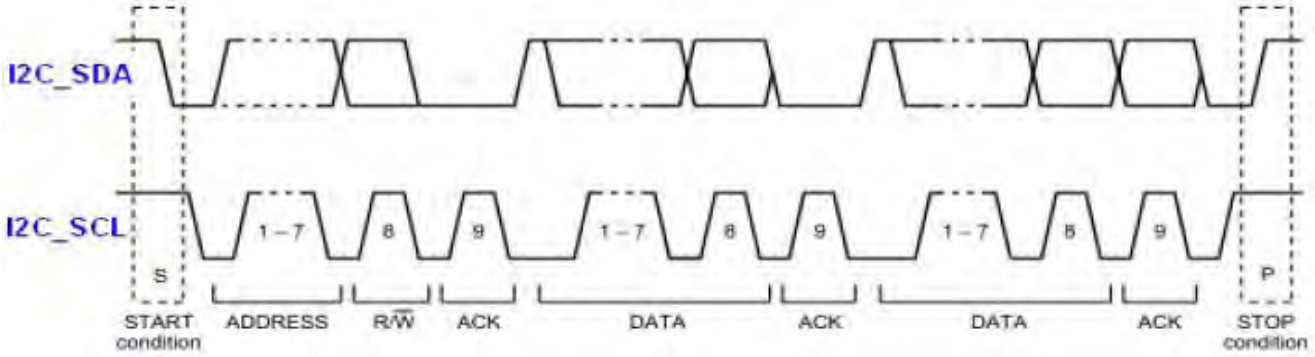
VCOM will change while VOCMIN change

Source output will change while LD signal falling edge.



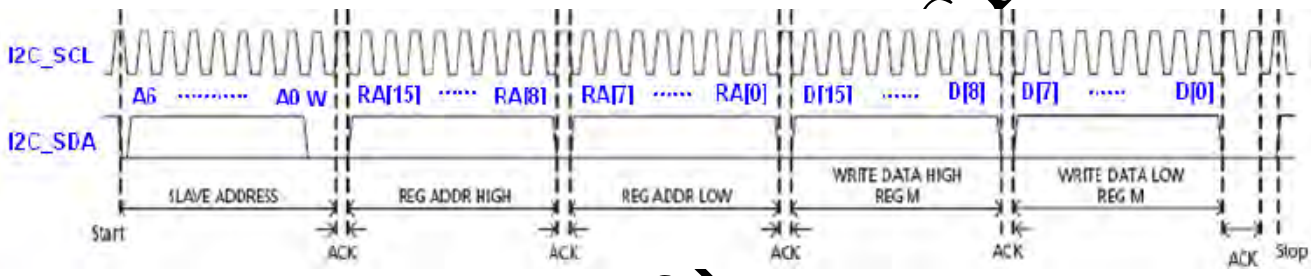
5. Touch panel timing

5.1. I2C Timing Diagram

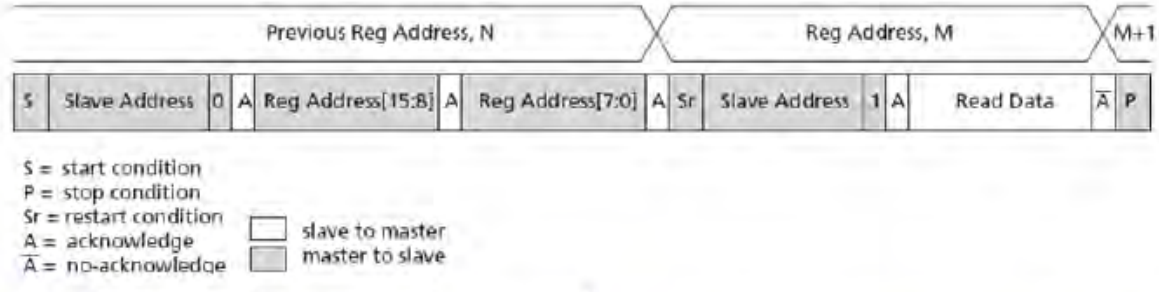


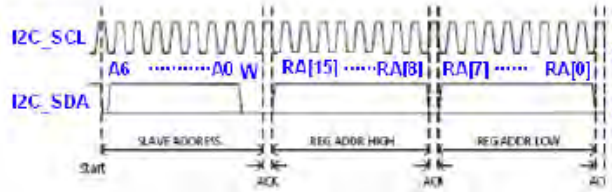
Note : Slave address is 1001100.

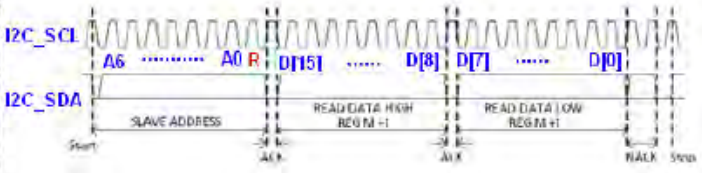
5.2. Register Write Sequence



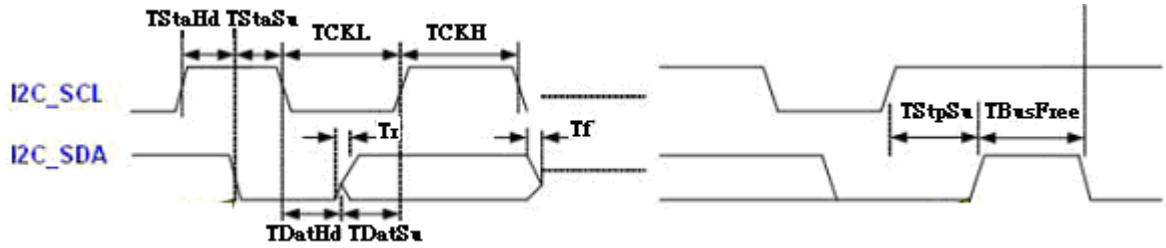
5.3. Register Read Sequence







5.4. I2C Timing Characteristics



VDDI=1.65~3.3V, VCI=2.5~3.3V, TA=25℃

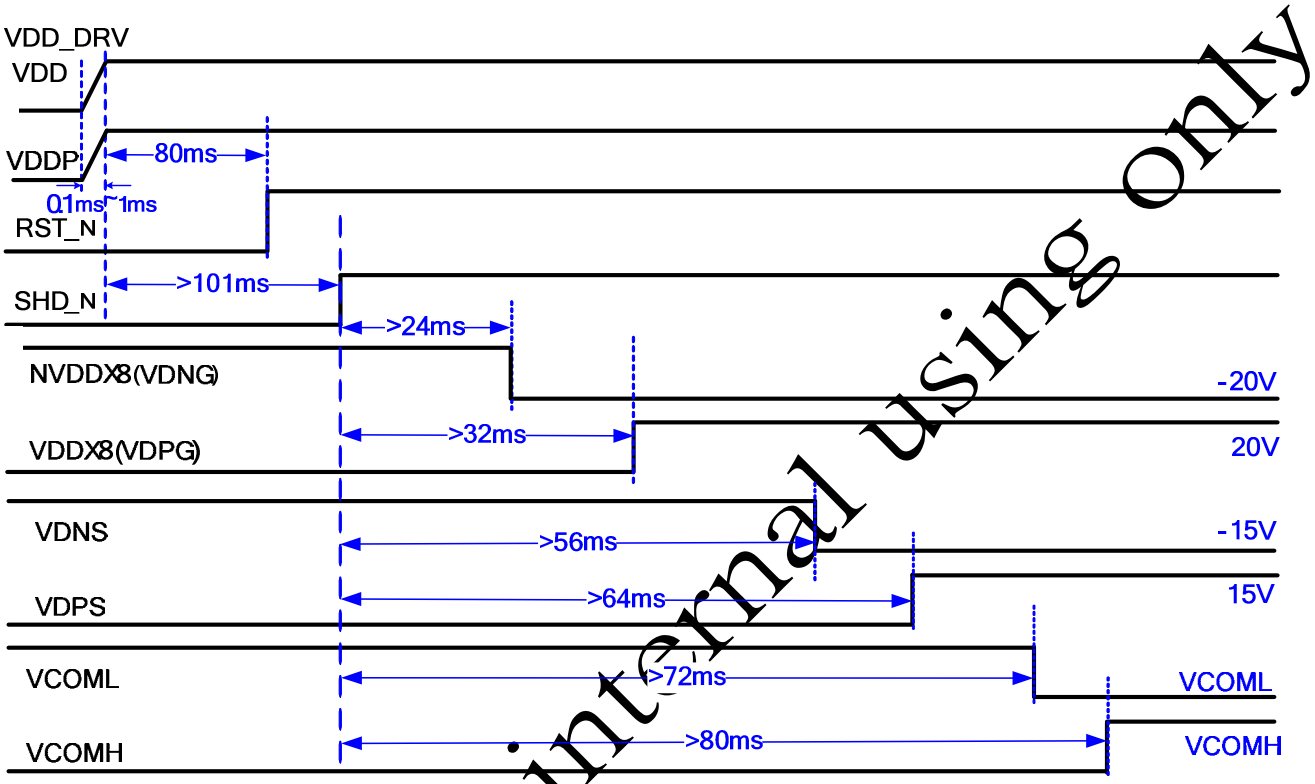
Item	Symbol	Min.	Typ.	Max.	Unit
Working Frequency	Fclk	-	-	400	KHz
I2C Clock Low	TckL	1250	-	-	ns
I2C Clock High	TckH	1250	-	-	ns
I2C Data ring time	Tr	-	-	300	ns
I2C Data falling time	Tf	-	-	300	ns
I2C Data hold time	TDatHd	0	-	-	ns
I2C Data setup time	TDatSu	100	-	-	ns
I2C Start Condition hold time	TStaHd	600	-	-	ns
I2C Start Condition setup time	TStaSu	600	-	-	ns
I2C Stop Condition setup time	TStpSu	600	-	-	ns
I2C Bus free time	TBusFree	1300	-	-	ns

F. Power On/Off Characteristics

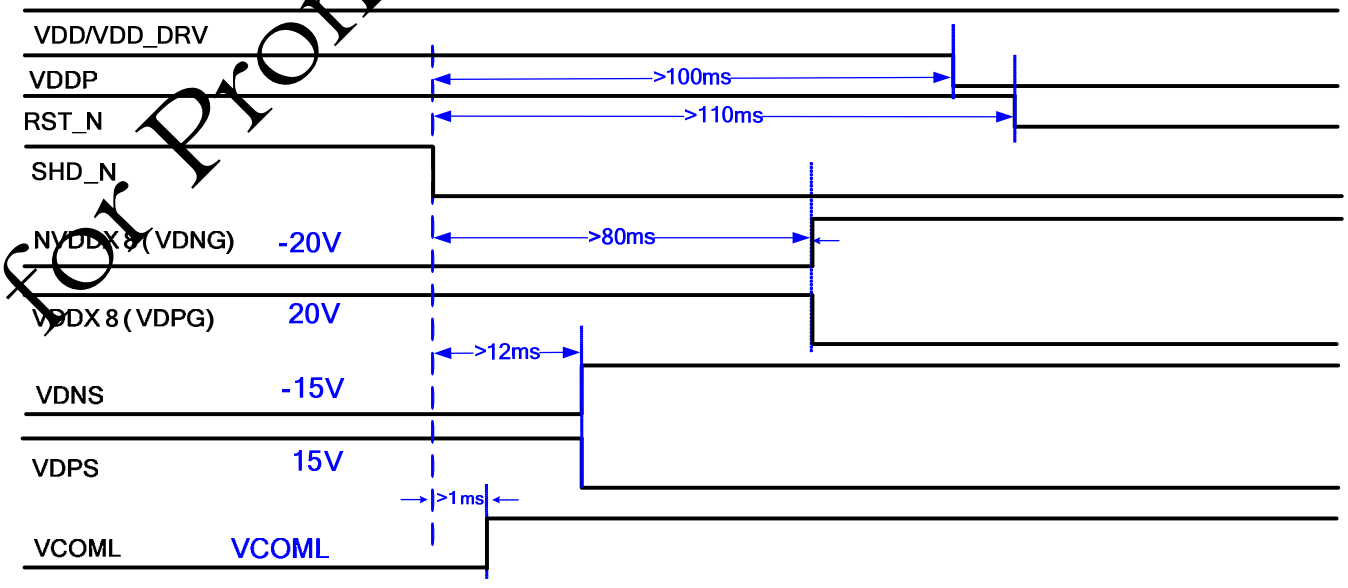
1. Recommended Power On/off Sequence

The suggested power on/off sequence is below:

1. Power on sequence:



2. Power off sequence:



G. Optical Specification

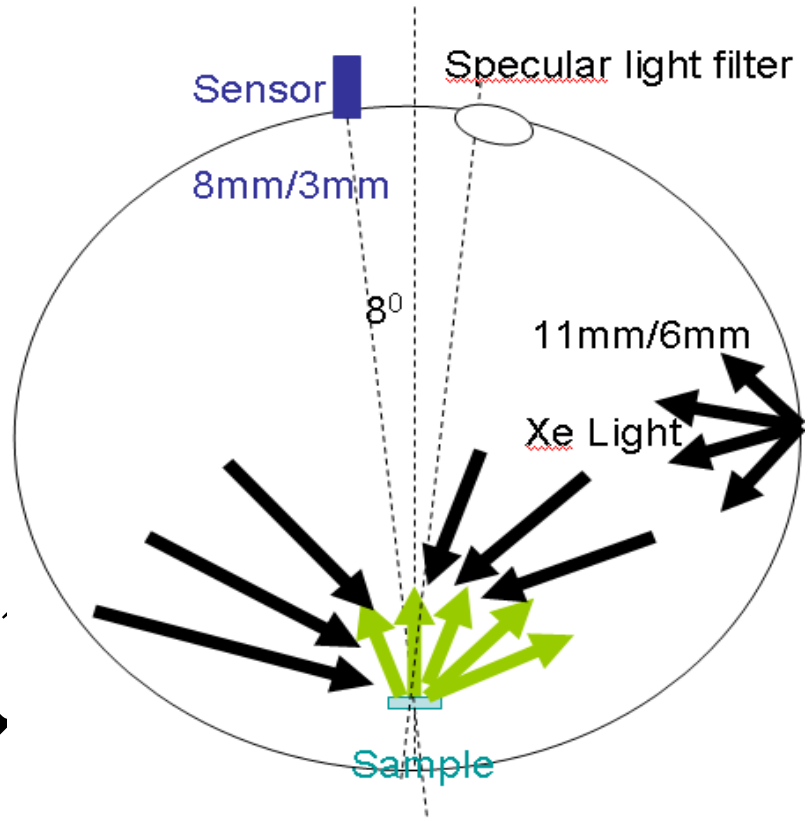
All optical specification is measured under typical condition (Note 1, 2)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Reflectance	R	white	24	26	--	%	Note1,2,3,4
Contrast Ratio	CR	At optimized viewing angle	4	5	--		Note1,2,3,5
Update Time	T	T=25℃ T=10℃ T=0℃	--	950 2310 2750	1010 2450 3150	ms	Note 3

Note 1. Ambient temperature =25℃

Note 2. Reflectance and constrast ratio are measured by KONICA MINOLTA spectrophotometer CM-2600d.

Note 3: The measurement shall be conducted under AUO specificed driving condition, including LUT and TCON codes.



Note 4. Definition of Reflectance:

The Reflectance is expressed as:

R = Reflectance Factor$_{\text{white board}}$ x (L_{center} / $L_{\text{white board}}$)

L_{center} is the luminance measured at center in a white area. $L_{\text{white board}}$ is the luminance of a standard white board.

Note 5. Definition of contrast ratio:

The contrast ratio (CR) is the ratio between the reflectance in a full white area (Rl) and reflectance in a dark area (Rd).

$$\text{Contrast ratio (CR)} = \frac{\text{Rl}}{\text{Rd}}$$

H. Reliability Test Items

	Test	Condition	Condition	Remark
1	High-Temperature Operation	Tamb=+50℃, RH=30% for 240hrs	IEC 60068-2-2Bp	Update pattern four times per minute.
2	Low-Temperature Operation	Tamb=0℃ for 240hrs	IEC 60068-2-2Ab	Update pattern four times per minute.
3	High-Temperature Storage	Tamb=+70℃, RH=23% for 240hrs	IEC 60068-2-2Bp	
4	Low-Temperature Storage	Tamb=-25℃ for 240hrs	IEC 60068-2-2Ab	
5	High-Temperature, High-Humidity Operation	Tamb=+40℃, RH=90% for 168hrs	IEC 60068-2-3CA	Update pattern four times per minute.
6	High-Temperature, High-Humidity Storage	Tamb=+60℃, RH=80% for 240hrs	IEC 60068-2-3CA	
7	Temperature Cycle	1 Cycle：[-25° C 30min] -> [+70° C 30min]：100 cycles	IEC 60068-2-14	
8	UV Exposure Resistance	Condition: 1120W/m2, 40℃ Test Duration: 3 cycles (Definition of 1 cycle: 8 hr at exposure state and 16Hr at non-exposure state)	IEC 60068-2-5Sa	
9	Package Vibration	1.04G, Frequency : 10 ~ 500HZ Direction : X, Y, Z Duration : 1 hours in each direction		
10	Package Drop Impact	Drop from height of 100 cm on concrete surface. Drop sequence : 1 corner, 3 edges, 6 faces one drop for each.		
11	Electrostatic discharge	Air-mode : +/- 8kV Contact-mode : +/- 4kV	IEC 61000-4-2	
12	Altitude test Operation	700hPa(=3,000m) 48hrs		
13	Altitude test Storage	260hPa(=10,000m) 48hrs		

14	**FPC Bonding Strength**	**Pull the FPC Stiffener part with a force of 500gf in the horizontal and vertical directions**		
15	**FPC bending Performance**	**Apply MIT method. Bending rate radius：1.0mm Weight 500gf, Bending angle：±135° Bending cycle：20 times**		
16	**Stylus Tapping**	**POLYACETAL Pen：Top R0.8mm Load：300gf Speed：3 times/sec Total 13,500 times**		**Pass criteria - no glass breakage or damage to micro-cups**

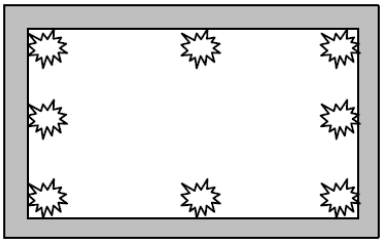
Note 1. In the above conditions, there is no display function NG issue occurred. All the cosmetic specification is judged before the reliability stress.

Note 2. The test modules will be kept at 25℃ environment for 4 hours after finish the environmental test and make measurement after AUO specified TCON code and waveform re-driving. The judgement of above tests should satisfy minimum contrast ratio and minimum reflectance.

Note 3. For Item 10, in addition tosatisfy minimum contrast ratio and minimum reflectance, the display shall be able to identify 4 gray levels, including Black and White when being driven under AUO specified driving condition at the end of test.

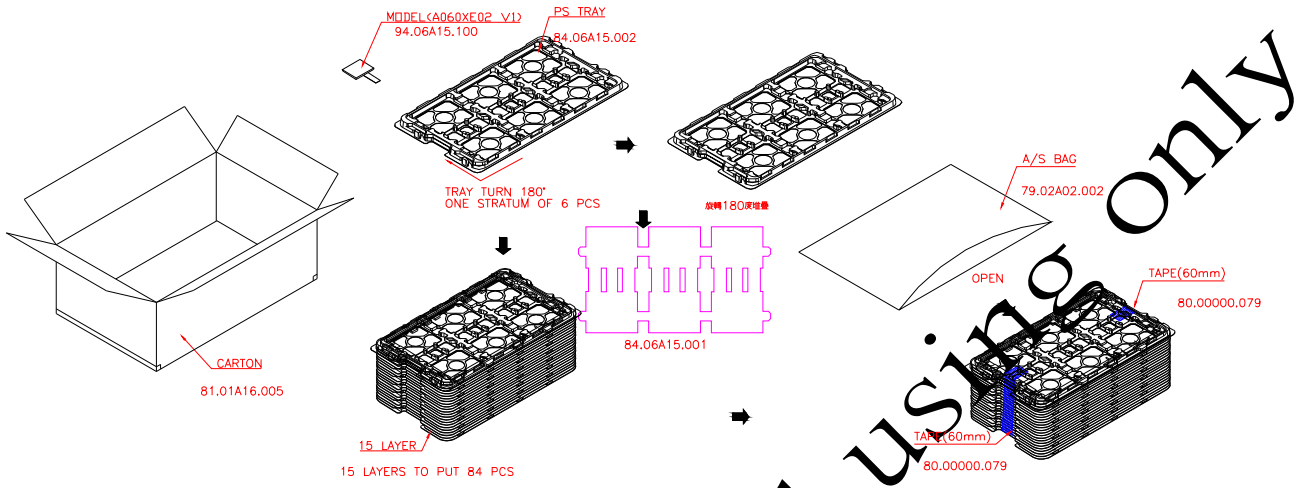
Note 4. ESD testing method.

1. Ambient: 24~26℃, 56~65%RH, atmospheric pressure : 940~960hPa
2. Instruments:NoisekenESS-2000,
3. Operation System: AUO pattern generator
4. Test Mode: Non-operating mode, test pattern: chess
5. Test Method:
   a. Contact Discharge: 150pF(330Ω) 1sec, 8 points, 25 times/point
   b. Air Discharge: 150pF(330Ω) 1sec, 8 points, 25 times/point
6. Test point:

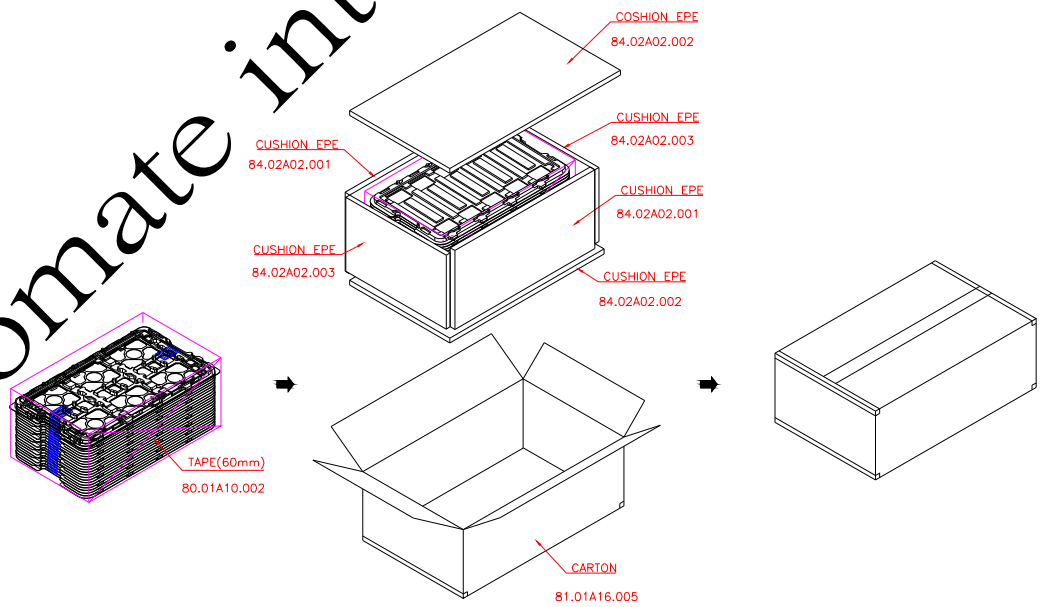


I. Packing and Marking

1. Packing Form

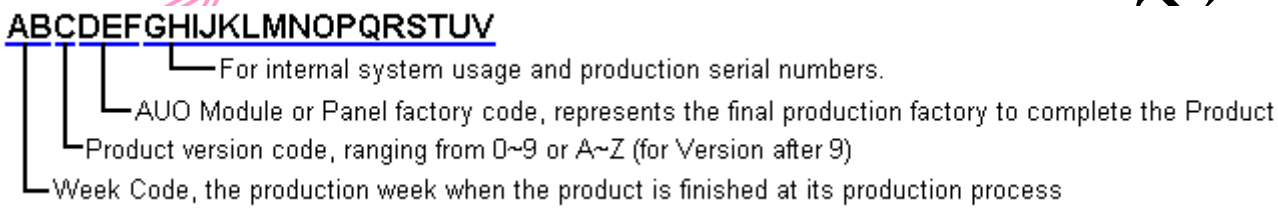


MAX. CAPACITY:84 MODULES
MAX. WEIGHT:TBD kg
MEAS. 600 x 353 x 210 mm



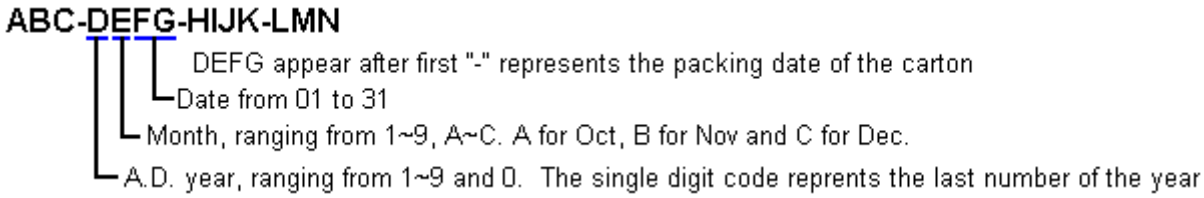
2. Module/Panel Label Information

The module/panel (collectively called as the “Product”) will be attached with a label of Shipping Number which represents the identification of the Product at a specific location. Refer to the Product outline drawing for detailed location and size of the label. The label is composed of a 22-digit serial number and printed with code 39/128 with the following definition:



3. Carton Label Information

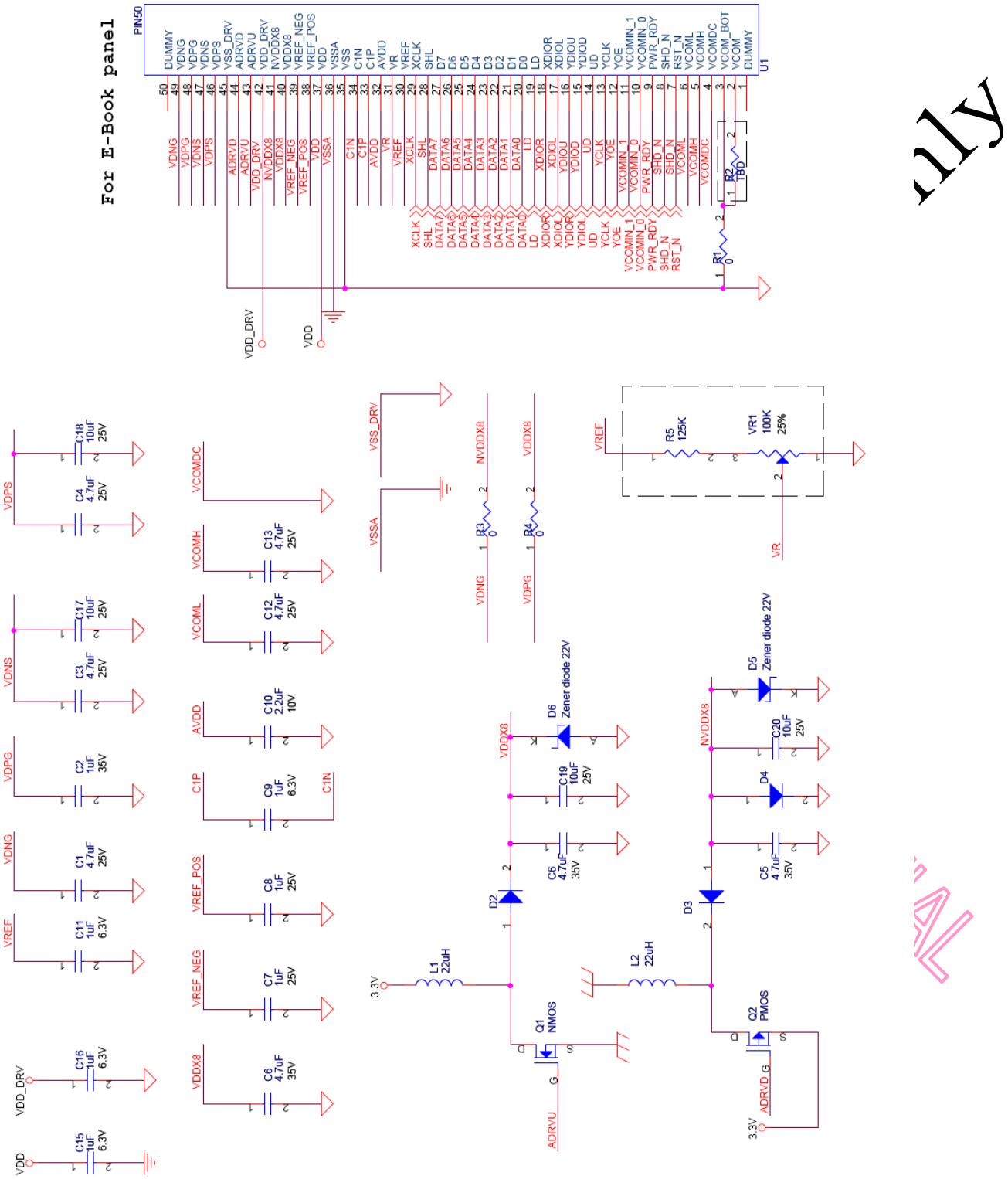
The packing carton will be attached with a carton label where packing Q’ty, AUO Model Name, AUO Part Number, Customer Part Number (Optional) and a series of Carton Number in 13 or 14 digits are printed. The Carton Number is appearing in the following format:



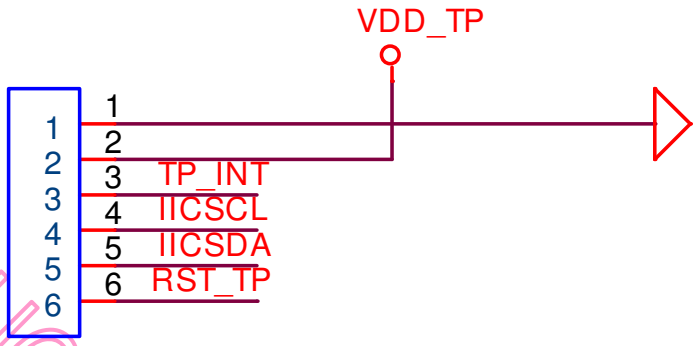
Refer to the drawing of packing format for the location and size of the carton label.

J. Application Note

1. Application Circuit



2. Touch panel pin assign circuit



K. Precautions

1. Do not twist or bend the module and prevent the unsuitable external force for display module during assembly.
2. Adopt measures for good heat radiation. Be sure to use the module with in the specified temperature.
3. Avoid dust or oil mist during assembly.
4. Follow the correct power sequence while operating. Do not apply the invalid signal, otherwise, it will cause improper shut down and damage the module.
5. Less EMI: it will be more safety and less noise.
6. Please operate module in suitable temperature. The response time & brightness will drift by different temperature.
7. Be sure to turn off the power when connecting or disconnecting the circuit.
8. Display surface never likes dirt or stains.
9. A dewdrop may lead to destruction. Please wipe off any moisture before using module.
10. High temperature and humidity may degrade performance. Please do not expose the module to the direct sunlight and so on.
11. Acetic acid or chlorine compounds are not friends with display module.
12. Static electricity will damage the module, please do not touch the module without any grounded device.
13. Do not disassemble and reassemble the module by self.
14. Be careful do not touch the rear side directly.
15. No strong vibration or shock. It will cause module broken.
16. Storage the modules in suitable environment with regular packing.
17. Be careful of injury from a broken display module.
18. Please avoid the pressure adding to the surface (front or rear side) of modules, because it will cause the display non-uniformity or other function issue.
19. Application under direct sunlight is strongly not recommended as it would result in display performance degradation.
20. It is highly recommended that the display is exposed to an even lighting condition to ensure a good display uniformity.
21. Elimination of light exposure to the display by applying proper means, e.g. lighting shielding cover is suggested when the display is not being used to extend the life performance of the device.
22. Heat isolation or heat sink to control uniformity of panel temperature should smaller than 1℃
23. Any performance degradation or display distortion which can be eliminated by display refreshing should not be regarded as a defect

L. Touch Panel Command and Register Map

1. I2C Protocol Definition

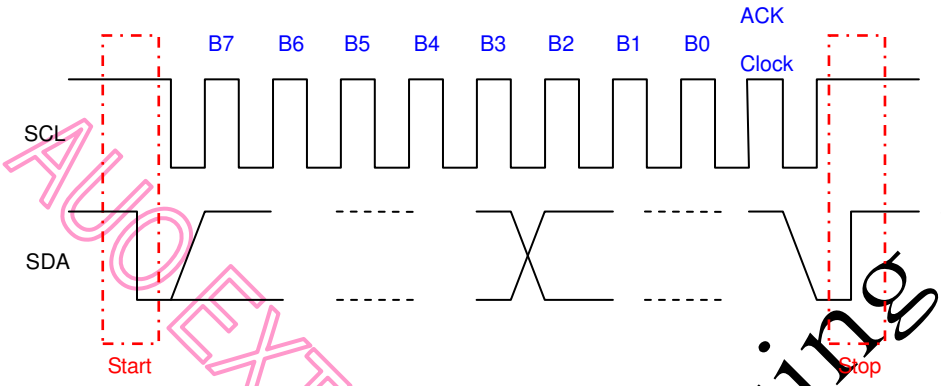


Figure 1. Standard I^2C Transaction Unit

The sensor controller supports standard I^2C protocol with SCL up to 400KHz. The device address is 0x5C. The chip also provides both single and sequential access. Figure 2 shows the write operation using single or sequential mode. Figure 3 also depicts the standard I2C transaction for single for sequential read mechanism.

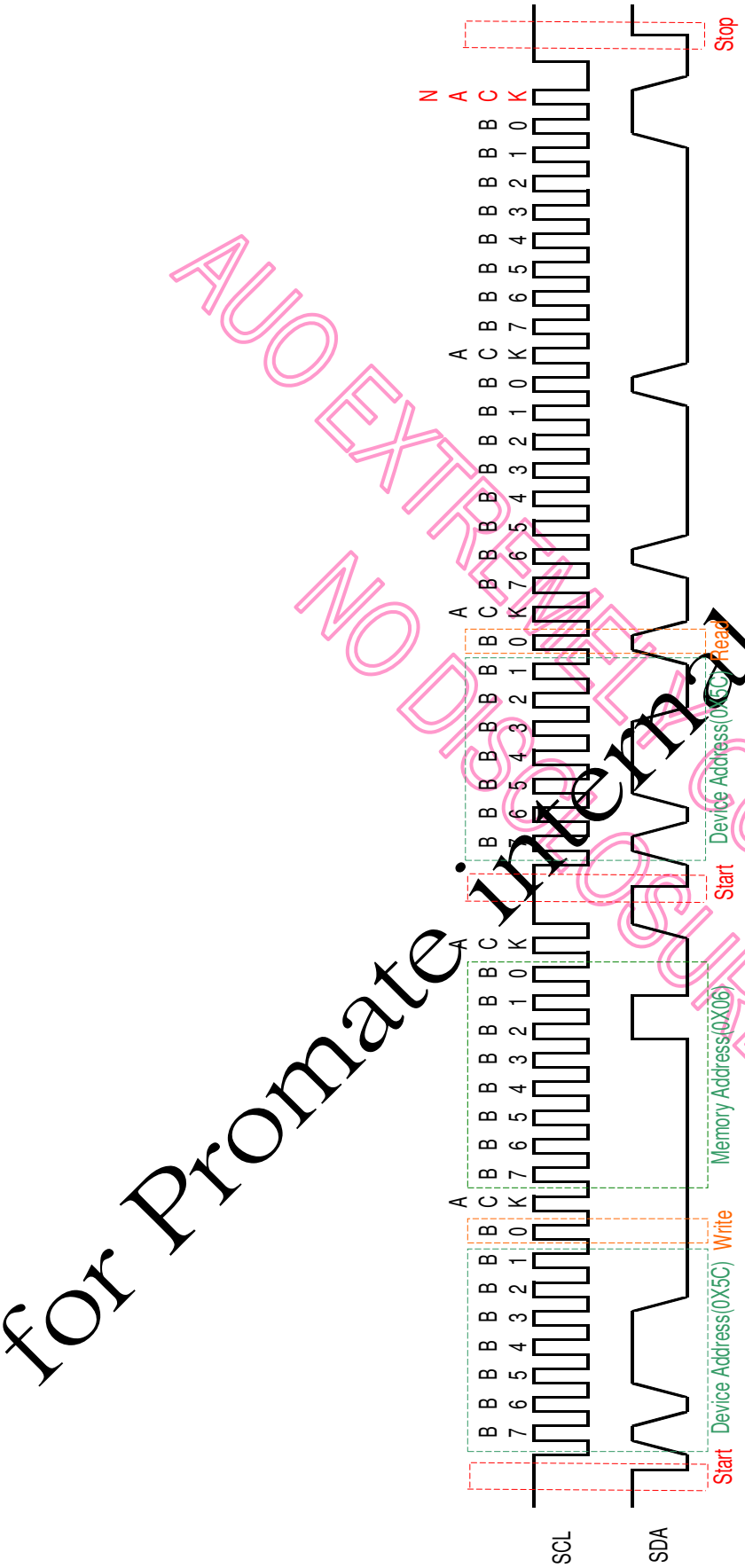
Write Operation															
Single	Start	Device Address (W)	A	Mem Addr	A	Data[0]	A	Stop							
Sequential	Start	Device Address (W)	A	Mem Addr	A	Data[0]	A	Data[1]	A	.....	A	Data[n]	A	Stop	

Figure 2. Write Operation with Single/Multiply Access

Read Operation															
Single	Start	Device Address (W)	A	Mem Addr	A	Start	Device Address (R)	A	Data[0]	NA	Stop				
Sequential	Start	Device Address (W)	A	Mem Addr	A	Start	Device Address (R)	A	Data[0]	A	.....	A	Data[n]	NA	Stop

Figure 3. Read Operation with Single/Multiply Acce

Suppose the Y[3] raw data is 321. If only Y[3] is read, user should issue the waveform as following:



2. Coordinate Register Map

Addr.	Addr.(HEX)	Description	R/W	B7	B6	B5	B4	B3	B2	B1	B0
0	00	X1 (LSB)	R	X1[7]	X1[6]	X1[5]	X1[4]	X1[3]	X1[2]	X1[1]	X1[0]
1	01	X1 (MSB)	R	0	0	0	0	0	0	X1[9]	X1[8]
2	02	Y1 (LSB)	R	Y1[7]	Y1[6]	Y1[5]	Y1[4]	Y1[3]	Y1[2]	Y1[1]	Y1[0]
3	03	Y1 (MSB)	R	0	0	0	0	0	0	Y1[9]	Y1[8]

Note: (1) (X1, Y1) means the touched point

(2) The coordinate of X1 = X1(LSB) + X1(MSB)*256, Y1 = Y1(LSB) + Y1(MSB)*256

(3) If no touch, (X1, Y1)=(0,0)

3. Display and Touch Resolution

If screen resolution (blue) is 800x600 , and touch resolution (yellow) is the same (800x600)

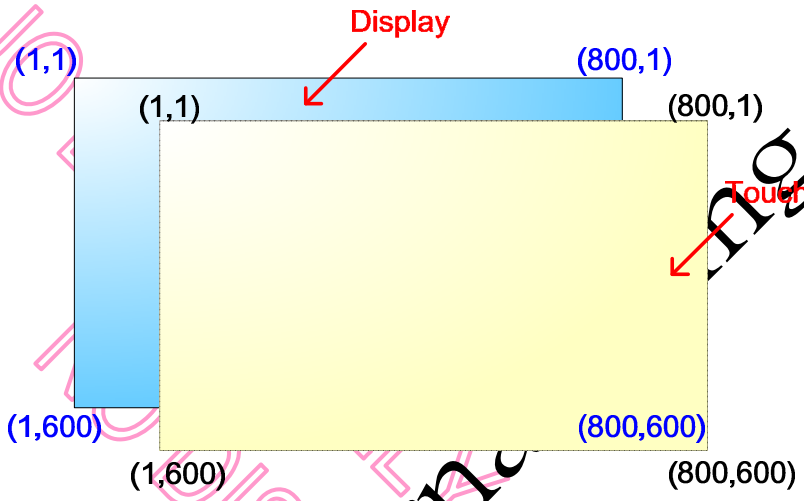
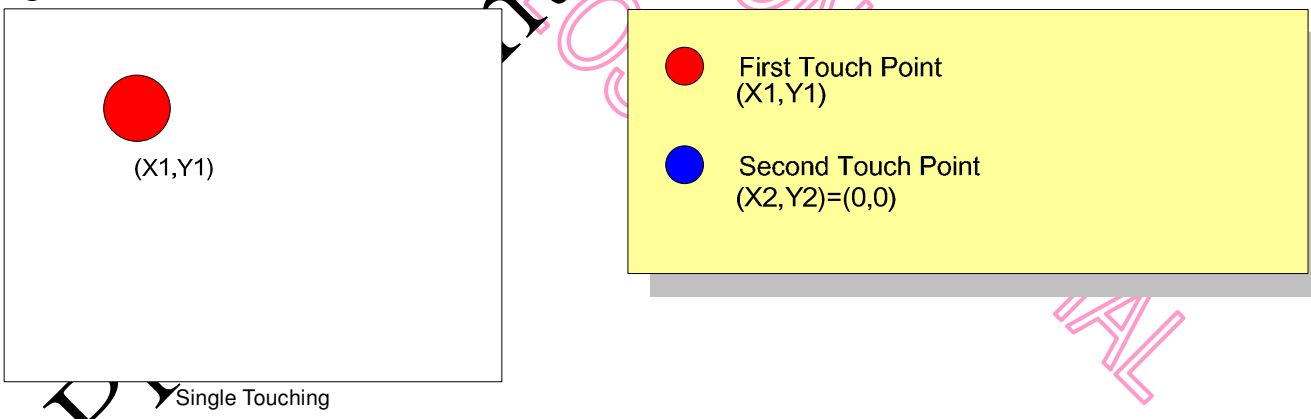


Figure 5 Reference of touched point diagram

4. Single Touch



Single Touching

5. Sensitivity

Addr.	Addr.(HEX)	Description	R/W	B7	B6	B5	B4	B3	B2	B1	B0
111	6F	X_SENSITIVITY (THRESHOLD)	R/W	X_SENSITIVITY[7:0]							
112	70	Y_SENSITIVITY (THRESHOLD)	R/W	Y_SENSITIVITY[7:0]							

Note: (1) The default value for X/Y SENSITIVITY is 0X14

6. Interrupt Operation Mode

This chip should support both polling and interrupt way to get the coordinate and raw data by I2C interface. The figure below depicts the interruption operation.

6.1 Interrupt Mode Setting

Addr.	Addr.(HEX)	Description	R/W	B7	B6	B5	B4	B3	B2	B1	B0
113	71	INT_SETTING	R/W	TP_NUM[2]	TP_NUM[1]	TP_NUM[0]	INT_RELEASE	EN_INT	INT_POL	INT_MODE[1]	INT_MODE[0]
114	72	INT_WIDTH	R/W	INT_WIDTH[7:0]							

Note:

(1)TP_NUM[2:0] :TP_NUM means how many fingers touched on the panel

000: No finger 001: One finger

010: Two fingers others: reserved

(2) INT_RELEASE

Under Touch Periodical Mode, once the behaviour of finger touched and then left was established, sensing IC will stop to scan until INT_RELEASE be modified INT_RELEASE default is 0

(3) EN_INT

0: Disable interrupt 1: Enable interrupt

(4) INT_POL

0: The interrupt is low-active(default) 1: the interrupt is high-active

(5) INT_ MODE[1:0]

00: INT assert periodically 01: INT assert only when coordinate difference

10: Touch Indicate(default) 11: INT assert only when INT_RELEASE be modified

(6) The default value for INT_SETTING is 0X0C; INT_WIDTH is 0X64

6.2 Sensing Periodical Mode (INT_MODE[1:0] = [0,0]).

For sensing periodical mode, the INT_MODE[1:0] should be [0,0].

The data must be ready (including coordinate and raw data) before signal 'INT' rising.

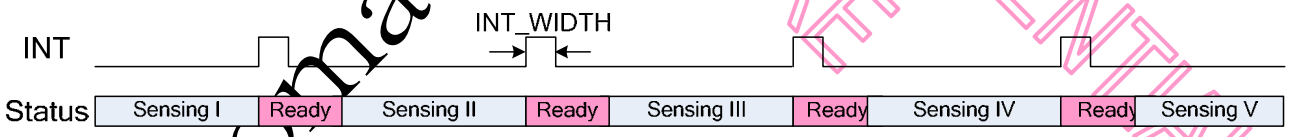


Figure 7: Interruption with INT_R auto-reset

6.3 Coordinate Compare Mode (INT_MODE[1:0] = [0,1]).

The INT signal will be asserted while coordinate changes under comparison mode (INT_MODE[1:0] = [0,1]).

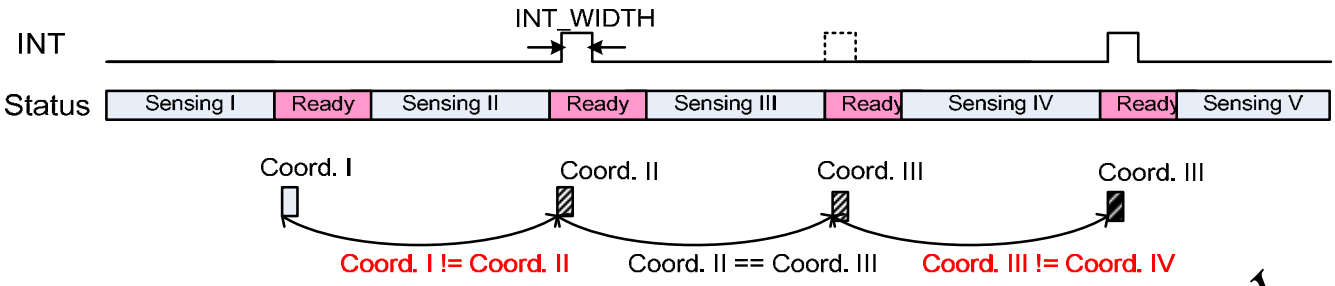


Figure 8: Interruption Flag under Coordinate Compare Mode

6.4 Touch Indicate Mode (INT_MODE[1:0] = [1,0]).

The interrupt will assert when the touch is valid. The interrupt should keep high until the touch is released.

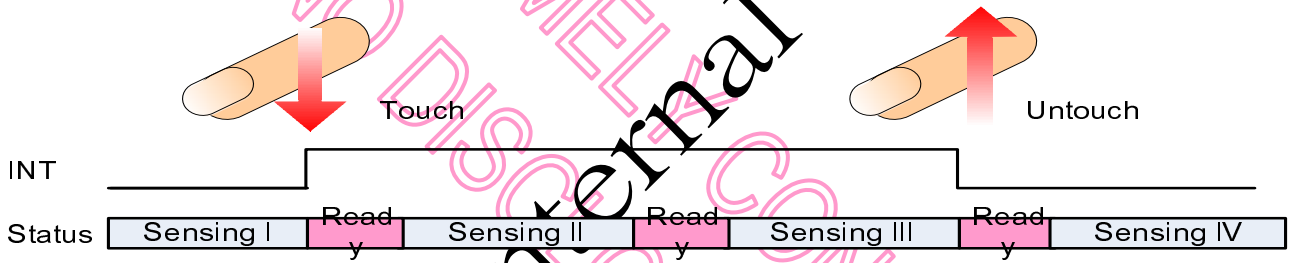
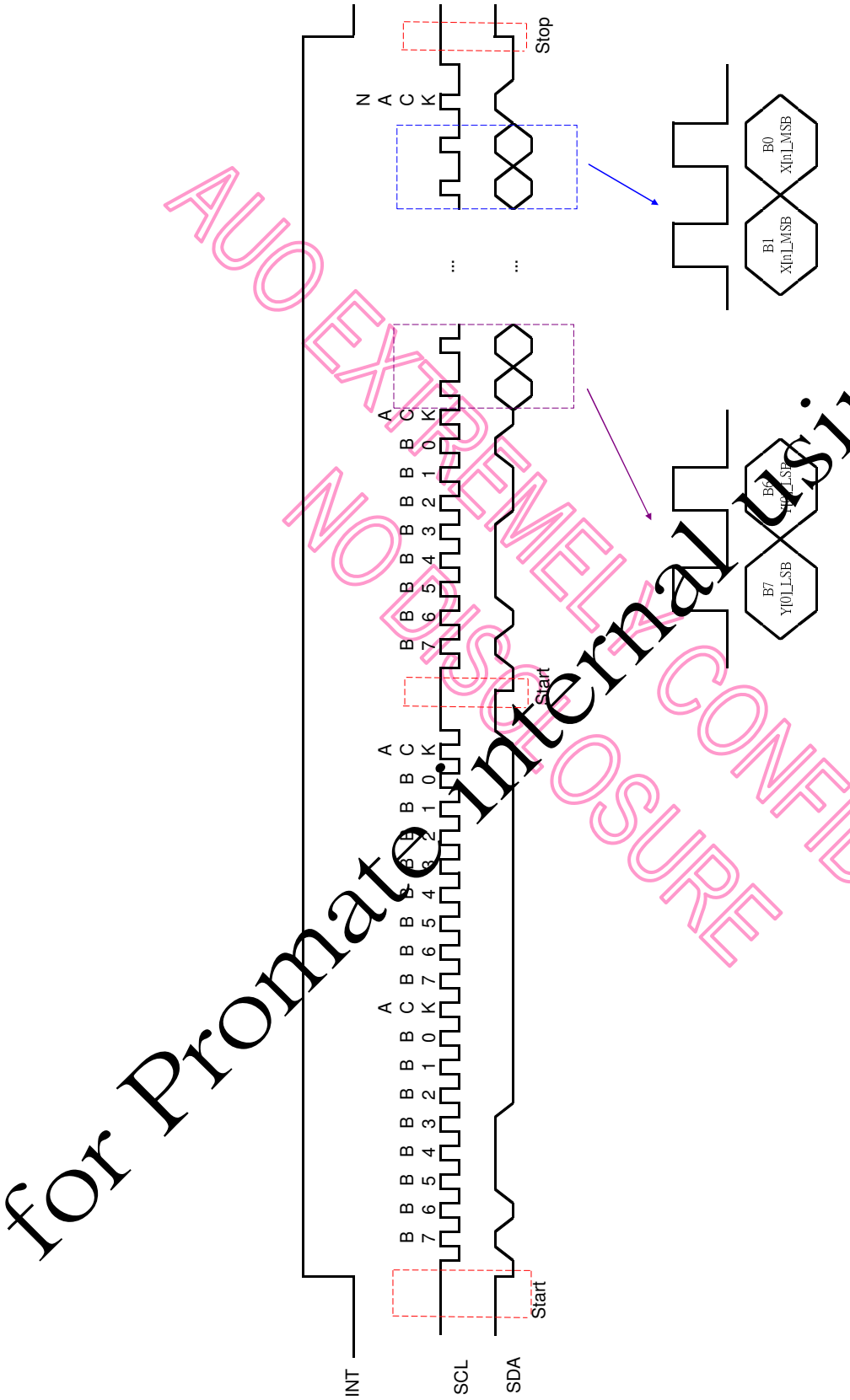


Figure 9: Touch Indicate Mode

Combination interrupt with I2C sequential read raw data operation for as following (for INT_MODE[1:0] = [1,0])



7. Power Mode

Addr.	Addr.(HEX)	Description	R/W	B7	B6	B5	B4	B3	B2	B1	B0
115	73	Power Mode	R/W	IDLE_PERIOD[3]	IDLE_PERIOD[2]	IDLE_PERIOD[1]	IDLE_PERIOD[0]	0	ALLOW_SLEEP	POWER_MODE[1]	POWER_MODE[0]

The capacitive sensor controller support 3 steps of power saving: Active, Sleep, Deep Sleep, the following section describe relative scan rate and power consumption:

The default value is 0X50

Active Mode:

The scan speed will reach 60Hz, this mode makes full-speed sensing and data process to provide best performance. the Power Mode is '0'.

Sleep Mode:

This mode will lower the scan speed down to 10Hz. Active Mode can enter sleep mode automatically or by command. When the system issues a command to change power mode to '1', the scan rate will switch to 10Hz at next scan cycle. When allow_sleep parameter is given, and user don't touch the screen longer than IDLE_PERIOD ms. the controller should also enter sleep mode directly and change the scan rate to 10 Hz immediately.

When user touches the screen in **active region**, the controller should return to Active mode. besides, when system assert a command to change the power mode to '0', the scan rate should also rise to 60Hz.

Deep Sleep Mode:

When the chip enter deep sleep mode, the scan speed will reduce to 1Hz to achieve minimum power consumption. While deep sleep mode, all the registers are accessible during 4 ms, and it start from end of interrupt transition. The figure 13 and figure 14 shows a example to reference.

The only way to leave/enter deep sleep mode is change the power mode by specific command. The power mode is defined as '2'

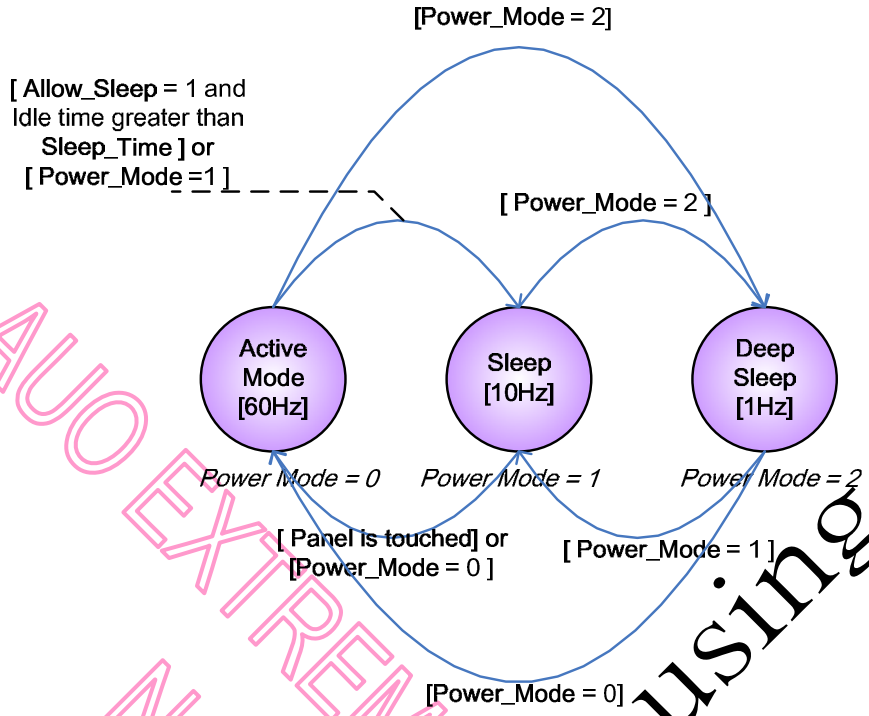


Figure 10 Power Mode Diagram

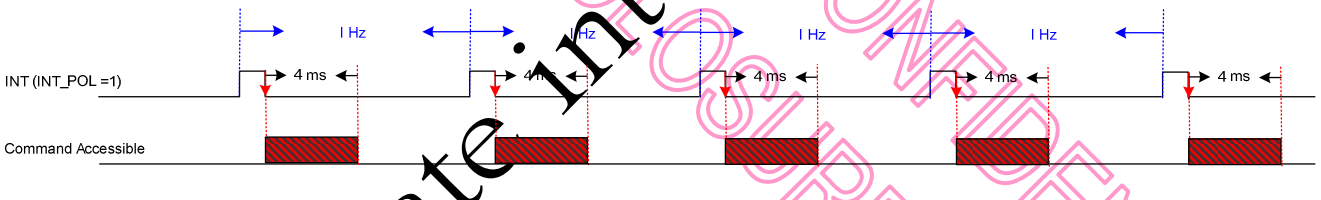


Figure 11 Command Accessible in Deep Sleep Mode (INT_POL=1)

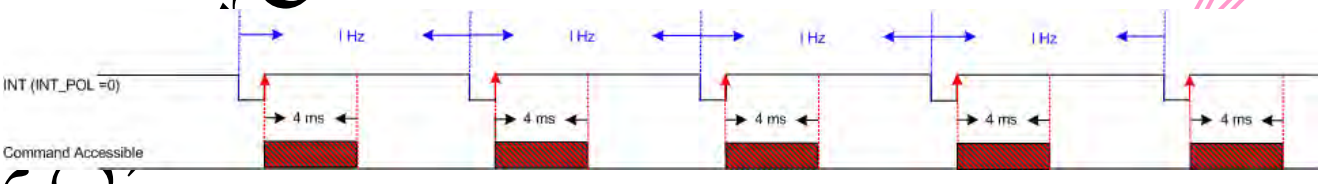


Figure 12 Command Accessible in Deep Sleep Mode (INT_POL=0)

8. Calibration

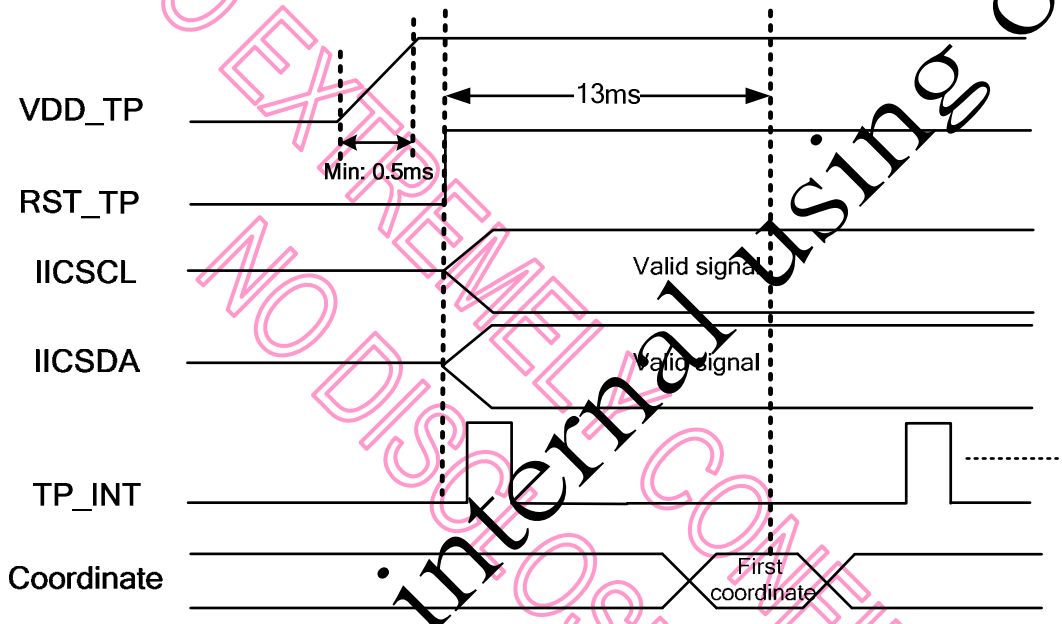
Addr.	Addr.(HEX)	Description	R/W	B7	B6	B5	B4	B3	B2	B1	B0
120	78	Calibration	W	0	0	0	0	0	0	1	1

"Calibration" procedure has to do once after assembly

Set address 0x78 as a 0x03 and wait 500ms, "Calibration" procedure will be done

9. Power On/Off Sequence

9.1 power on sequence



9.2 power off sequence